

# Optimization of Front-End Design in Imaging and Spectrometry Applications With Room Temperature Semiconductor Detectors

L. Fabris\*, P.F. Manfredi

**Abstract**--This paper addresses the optimization of front-end design in position sensing, imaging and high-resolution energy dispersive analysis with room temperature semiconductor detectors. The focus will be on monolithic solutions able to meet the requirements of high functional density set by multielectrode, finely segmented detectors. Noise will be an issue of dominant importance in all the analysis developed here. It will be shown that the front-end optimization process requires two subsequent steps. One is the choice of the technology. The most advanced CMOS processes featuring a short channel and a very thin gate oxide will be evaluated along with technologies that feature a Junction Field-Effect Transistor (JFET) as an input device. Once the technology and therefore the nature of the preamplifier input element is chosen, the second step is directed to optimizing the design of the input stage. This process requires that some criteria that have been used to this effect in the past and were restricted to the sole input element be revisited. It will be shown, indeed, in this paper that the optimization process, especially as far as noise is concerned, must take into account the fact that the preamplifier input stage is customarily a cascode and therefore the noise in the common gate element affects the optimization of geometry and working point of the input device. This consideration will be applied to the choice of the optimum aspect ratio and working point for either a CMOS or a JFET employed as front-end devices. Attention will be devoted in particular to the choice of the channel length in a CMOS design, a point that has acquired particular importance with the advent of submicron CMOS technologies. The discussion of practical design examples based on the previous considerations concludes the paper.

## I. SUMMARY

ROOM temperature semiconductor detectors made of different elements and compounds, Si, CdTe, HgI<sub>2</sub>, SiC<sub>4</sub> are presently being employed in highly diversified fields of investigation for position sensing and imaging of high spatial resolution and finely resolved energy dispersive spectrometry.

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\*Corresponding Author.

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L. Fabris is with E. O. Lawrence Berkeley National Laboratory, Berkeley, CA 94720, USA (telephone: 510-486-6867, e-mail: LFabris@lbl.gov)

P.F. Manfredi is with E. O. Lawrence Berkeley National Laboratory, Berkeley, CA 94720, USA (telephone: 510-486-7786, e-mail: PFManfredi@lbl.gov), Pavia University, Via Ferrata 1 – 27100 Pavia (Italy) and INFN Pavia, Via Bassi – 27100 Pavia (Italy).

Some of these applications require highly segmented multielectrode configurations, like pixel and microstrip detectors. This brings about the need for front-end systems of high functional density, which can be met only by a monolithic front-end design. The monolithic design is a mandatory solution also in applications where the detector segmentation is not extremely fine, but the total number of signal acquisition and processing channels is large. In most of applications noise is an issue of paramount importance. The counting rate capability is acquiring more and more importance as required in some cases of medical imaging and in the expanding applications of solid state imaging detectors in experiments at light sources. Radiation resistance in the front-end design is becoming an additional requirement in some situations.

The optimization of the front-end design becomes a fundamental aspect in the detector utilization. The choice of the front-end solution is driven by the nature of the detector, the compromise between noise and counting rate requirements and by possible additional features like, for instance, radiation hardness.

Two basic technologies are considered here, that differ for the type of front-end device they make available, either a MOSFET or a JFET. The CMOS processes are gaining favor by virtue of the recent advances that have brought the channel length well into the submicron region and the gate oxide thickness below 10 nm [1], [2]. Particularly the latter feature has resulted in a marked improvement in the noise behavior, as it has consistently reduced the 1/f term, which is a major limitation in low noise applications of MOSFETs [3], [4].

This is especially true for the P-channel device, which is the preferred choice when noise is an issue. Processes featuring a JFET as a front-end device are still the best solutions in high-resolution spectrometry [4], [5]. The JFET is superior to the PMOS in its noise behavior in the low-frequency region, which makes the JFET the most advisable choice when the lowest noise limits are to be attained by increasing the signal processing time. Just for the sake of pointing out the relative merits of MOSFETs and JFETs in low noise applications, fig. 1 compares the spectral densities of the channel noise in a PMOS, fig. 1 (a) and in an NJFET, fig. 1 (b). The curves refer to two devices for which aspect ratios and standing currents  $I$  are such to give the same

$(W/L) \times I$  value. The superior noise behavior of the JFET in the low frequency region is apparent. A JFET technology, however, cannot reach functional densities comparable to those of a CMOS process.

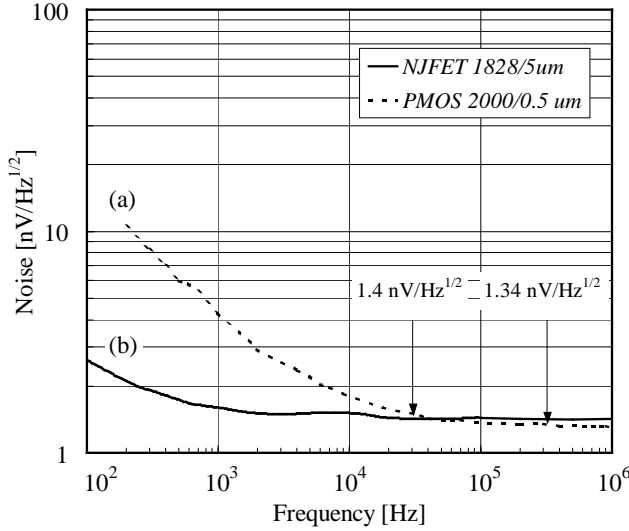


Fig. 1: Spectral densities of the input referred channel noise as a function of frequency (a) PMOS (b) NJFET, parts of monolithic processes.

The considerations about the choice of the technology can be concisely summarized by stating that CMOS processes are a mandatory solution when a high functional density on the chip is a dominant issue. With pixel detectors, where the electrode capacitances are small, and some compromise on noise can be accepted to enhance the rate capability, an NMOS input element is probably the best solution. With microstrip detectors, where the electrode capacitances are substantially larger and the channel noise of the input device becomes more important, a PMOS input element is advisable. When the noise limits are to be attained on a broad range of shaping times, the JFET is the first order solution.

Once the nature of the input device is fixed, the second step in the front-end optimization is relevant to the input active device in the preamplifier. It is to be pointed out that the choice of geometry and operating condition of the input active device done with the aim of optimizing the Equivalent Noise Charge (ENC) cannot disregard, as it is frequently done, the fact that the input device is part of a cascode (fig.2). The channel noise of the common gate transistor  $T_2$ , represented by the voltage source  $e_2$  in fig.2 may bring about a non-negligible contribution to ENC.

The extent to which  $e_2$  contributes to ENC and the mechanisms by which it affects the design of  $T_1$  will be discussed with reference to the charge-sensitive preamplifier model of fig.2, where the input cascode has been highlighted. In fig. 2,  $Q_i(t)$  is the detector signal and  $C_D$  the detector capacitance. The input transistor  $T_1$  is described by the voltage-controlled current source  $g_{m1}V_1$  in parallel to the dynamic drain-source resistance  $r_{o1}$ .  $C_{GS}$  and  $C_{GD}$  are the gate-

to-source and gate-to-drain capacitances of  $T_1$ , and its channel noise is accounted for by the current source  $i_{N1}$ .

The dc current sources  $I_{d1}$  and  $I_{d2}$  are shown for the sake of completeness in the description of the charge-sensitive preamplifier, whose signal path out of the input cascode is completed by the unity gain follower "1" and by the return path through the integrating capacitance  $C_f$ .

This paper will show how the presence of  $e_2$  alters the so called "capacitive matching" condition. It will then discuss the compromises that are to be made in the choice of the gate length  $L$  of  $T_1$  and of its standing current  $I$ . Both  $L$  and  $I$  control the transconductance of  $T_1$  and therefore its channel thermal noise. However, measures aiming at increasing  $g_{m1}$  by reducing  $L$  or increasing  $I$  clash with the enhanced ENC contribution by  $e_2$  resulting from the decrease in  $r_{o1}$ , which is a side-effect of either of these measures. These considerations become especially important nowadays, as related to the trend toward the reduction in the gate length of  $T_1$  demanded by the need of increasing its transition frequency.

The way the previous considerations are set to work will be illustrated in a practical design example of a preamplifier featuring a small JFET at the input, tailored to high-resolution energy dispersive analysis.

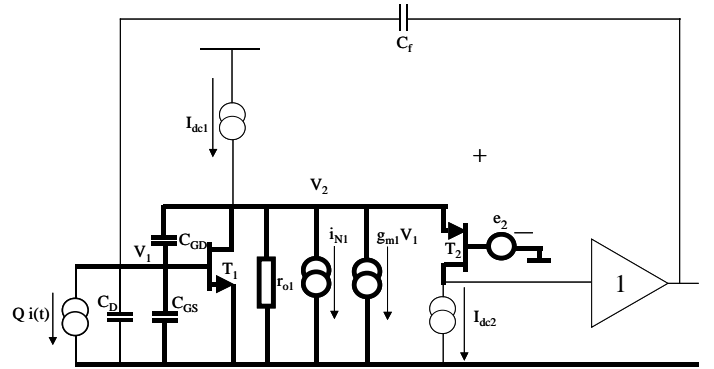


Fig. 2: Model of charge-sensitive preamplifier.

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